CLAIMS:

1. A bit-flipping sigma-delta modulator for a class D amplifier and comprising:

a quantiser coupled to a bit-flipping means; one or more look-ahead quantisers; and a controller having inputs from the quantiser and the look-ahead quantiser and arranged to enable the bit-flipping means to provide a different output from that of the quantiser in order to reduce the quantised output transition rate of the modulator;

a feedback circuit arranged to add a portion of the quantiser output to the input signal path of the modulator, and further comprising an integrator circuit in the input signal path between the input and the quantiser, the integrator circuit having a compensation circuit for adjusting the input to the quantiser when said previous modulator output has been changed by the bit flipping means from said previous quantiser output.

2. A modulator according to claim 1, said feedback circuit further arranged to add one or more additional portions of the quantiser output to the input signal path of the modulator, and further comprising one or more corresponding integrator circuits in the input signal path between the input and the quantiser, the integrator circuits each having a compensation circuit for adjusting the input to the quantiser when said previous quantiser output has been changed by the bit flipping means.

3. A modulator according to claim 1, said feedback circuit further arranged to add one or more additional portions of the output of the bit flipping means to the input signal path of the modulator, and further comprising one or more corresponding integrator circuits in the input signal path between the input and the quantiser.

4. A modulator according to claim 1 wherein said compensation circuit is arranged to adjust the input to the quantiser such that it is equivalent to a quantiser input having a feedback portion of a previous different output.

5. A modulator according to claim 4 wherein said compensation circuit is arranged to remove double said feedback portion from the input signal path when said previous quantiser output has been changed by the bit flipping means.

6. A modulator according to claim 1 wherein said feedback circuit is a multiple feedback filter circuit having multiple feedback paths from the output of the quantiser and having couplings to the inputs of the quantisers.

7. A modulator according to claim 1 wherein said modulator is a bi-level or tri-level modulator and when enabled said bit flipping means provides the or another state of the quantiser output as the different output.

8. A modulator according to claim 1 wherein said portion is provided by switchable predetermined coefficients, said switching controlled by the output of the quantiser.

9. A modulator according to claim 8 comprising a multiplexer coupled to an adder and arranged to switch between two coefficients depending on the output of the quantiser.

10. A modulator according to claim 1 wherein the compensating means comprises circuit means within the loop of a said integrator circuit to switchably add a compensation coefficient derived from said quantiser output.

11. A modulator according to claim 10 wherein the compensating means further comprises two switchable paths through the integrator loop, one of said paths comprising an adder to add said compensating coefficient, the coefficient and path depending on the output of the quantiser.

12. A modulator according to claim 1 further comprising a second look-ahead quantiser which determines the quantised output of said quantiser for the input sample two samples ahead, the controller further taking an input from said second look-ahead quantiser.

13. A modulator according to claim 1 wherein the controller comprises means for disabling the bit flipping means if the baseband noise resulting from enabling said bit flipping means is above a predetermined threshold.

14. A modulator according to claim 13 further comprising means for estimating the baseband noise as a result of enabling said bit flipping means, said estimate being dependent on the difference between the input of the quantiser and the output of the bit flipping means.

15. A modulator according to claim 14 wherein said noise estimate is dependant on the variance of the difference after baseband filtering.

16. A modulator according to claim 1 wherein the controller comprises:

a transition rate counter which provides a control signal when the transition rate of the quantised modulator outputs is above a predetermined level;

an alternation control which provides a control signal when consecutive said differences enabled by the bit flipping means are within a predetermined number of increases or decreases;

a transition control which provides a control signal when the inputs from the quantiser and look-ahead quantisers correspond to predetermined patterns;

wherein the controller enables the bit flipping means when a control signal is provided by the transition rate counter, the alternation control, and the transition control simultaneously.

17. A modulator according to claim 1 wherein the controller comprises:

a transition rate counter which provides a control signal when the transition rate of the quantised modulator outputs is above a predetermined level;

a weighted bit flipping control which provides a control signal when the baseband noise resulting from enabling said bit flipping means is below a predetermined threshold;

a transition control which provides a control signal when the inputs from the quantiser and look-ahead quantisers correspond to predetermined patterns;

wherein the controller enables the bit flipping means when a control signal is provided by the transition rate counter, the alternation control, and the transition control simultaneously.

18. A modulator according to claim 16 wherein the counter increments when there is no difference between current and previous quantiser output, and decrements by an amount dependent on the sampling frequency and maximum output transition rate when there is a difference between the current and previous quantiser output.

19. A modulator according to claim 18 wherein for a tri-level modulator, the decrement amount is doubled when the difference is between the highest and lowest outputs.

20. A modulator according to claim 16 wherein for a tri-level modulator, said predetermined patterns correspond to the previous quantiser output being equal to the look first ahead quantiser output and not equal to the current quantiser output, or the previous quantiser output not being equal to the current quantiser output and equal to the second look ahead quantiser output.

21. A class-D amplifier comprising a modulator according to claim 1.